Remarks/Arguments:

Claims 1 through 22 are presently pending. Claims 1-6, 8-12, 14-18, 21, and 22 stand rejected and claims 7, 13, 19, and 20 are objected to, but have been identified as allowable if rewritten in independent form. Applicant herein amends claims 1, 9, and 15. Support for the claim amendments can be found throughout the specification as originally filed. For example, see paragraphs 109 through 112 and Figures 16A-D. Applicant contends that no new matter is added. Applicant respectfully requests reconsideration in view of the above amendments and the following remarks.

Section 7 of the Office Action recites that "claims 1-6, 8-12, 14-18, 21-22 are rejected under 35 USC 103(a) as being unpatentable over Nystuen (2004/0088472) in view of Shiozaki et al. (4,683,533)." Claim 1 includes at least one feature that is not disclosed, taught, or suggested by Nystuen in view of Shiozaki. Claim 1 is directed to a memory controller and includes the following features (at least one of which is not found in the applied references):

> an arbiter configured to receive the memory requests from the plurality of requesters, the arbiter assigning a first memory request to a first processing path and a second memory request to a second processing path responsive to the memory banks requested by the received and assigned memory requests;
>
> a first path controller coupled to the arbiter and the plurality of memory banks, **the first path controller configured to process the first memory request in the first processing path to activate a first memory bank associated with the first memory request for a first data transfer;**
>
> a second path controller coupled to the arbiter and the plurality of memory banks, **the second path controller configured to process the second memory request in the second processing path to activate, during the first data transfer, a second memory bank associated with the second memory request for a second data transfer;**

This means that a first path controller processes a first memory request to activate a first memory bank for a first data transfer and a second path controller processes a second memory request to activate, during the first data transfer, a second memory bank for a second data transfer. Thus, the activation of the second memory bank for the second data transfer occurs after the activation of the first memory bank and during the first data transfer.

Section 5 of the Office Action recites that "Applicant's arguments filed June 27, 2006 have been fully considered but they are not persuasive." The Office Action further recites:

> Applicant's arguments appears as though the act of "a first path controller activating a first memory bank associated with a first memory request" occurs concurrently or simultaneously with "a second path controller processing a second memory request and a second process and path to activate a second memory." However, Examiner would like to point out that the claims simply recite "a first path activate a first memory bank associated with the first memory request; and a second path controller configured to process the second memory request in the second processing path to activate a second memory bank associated with the second memory request while the first memory bank is active" and the claims make no mention whatsoever the timing or order of these two operations. (Emphasis in original).

Applicant respectfully disagrees that there is no mention whatsoever of the timing or order of the two operations. Applicant contends that claim 1 clearly sets forth that the second memory bank is activated while the first memory bank is active. Thus, in order to satisfy this criteria, the first memory bank must be activated first followed by the activation of the second memory bank. Nonetheless, the applicant herein amends claim 1 to indicate that the activation of the first memory bank is for a first data transfer and that the activation of the second memory bank is for a second data transfer, and that the activation of the second memory bank occurs during the first data transfer. Accordingly, the activation of the first memory bank occurs before the activation of the second memory bank and is timed such that the activation of the second memory bank occurs during the first data transfer. Thus, applicant contends that claim 1 does mention timing and order of the activation requests.

The Office Action further recites that:

> Examiner would like to further mention that Nystuen discloses "a path controller for processing memory access requests to activate a first and second memory bank"; Abstract; and "processing memory requests to a first bank (bank 0) and a second bank (bank 1) where all banks are being precharged (activated) prior to processing the memory requests."

Applicant respectfully disagrees. The Office Action appears to equate precharge in Nystuen with activate. Applicant contends that this is incorrect. For example, see paragraphs 4 and 5 of Nystuen which recite:

> When performing write and read operations, the memory controller is responsible for generating the appropriate sequence of control signals for accessing the desired address in the memory device. This sequence typically involves precharging the columns in the bank to be accessed, activating the desired row within that bank and then writing to or reading from selected columns in the activated row.
>
> The memory cells at each column are coupled to a respective bit line (or pair of complementary bit lines). Each bit line has a voltage representing the data being read from or written to a memory cell in that column. A sense amplifier is coupled to each bit line (or pair of complementary bit lines) and has a latch for capturing the voltage on that bit line. A precharge command forces the sense amplifier and thus the bit line (or pair of bit lines) to a voltage level between a logic high value and a logic low value. After the bit lines in the memory array have bee precharged, the sense amplifiers are ready for an activate command. (Emphasis added.)

Additionally, see Table 1 of Nystuen in which activate commands and precharge commands are clearly differentiated. Accordingly, precharge and activation are not the same and, thus, Nystuen does not disclose activating a second bank while a first bank is active. Nevertheless, in order to facilitate prosecution, applicant herein amends claim 1, 9, and 15 to recite that the activation of the first memory bank is for a first data transfer and activation of the second memory bank is for a second data transfer, and that the activation of the second memory bank occurs during the first data transfer. This feature of claim 1 is neither disclosed, taught or suggested by Nystuen and Shiozaki et al., either alone or in combination. Accordingly, Applicant contends that claim 1 is allowable and respectfully requests withdrawal of the rejection.

Claims 9 and 15, while not identical to claim 1, include features similar to claim 1. Accordingly, applicant contends that claims 9 and 19 are also allowable.

Additionally, with respect to claims 17 and 21, the Office Action recites in response to applicant's argument that Nystuen fails to disclose, teach or suggest assigning a memory request to one of the at least one controllers from the plurality of memory requesters not in the grant history register using fixed priority logic that:

> Nystuen discloses "compare circuit 550 compares bank address stored in history register 512 and bank address presently received to determine whether either is to the same bank stored in register 512; and a *[sic]* each successive command is

> loaded, the corresponding bank address is loaded into the history register where the bank control circuit generates a bank precharge command if none of a predetermined number of memory access requests is to the memory bank; paragraphs 46-27; Abstract.

Applicant respectfully disagrees that Nystuen discloses, teaches, or suggests the claimed invention. The history register 512 identified as being present in Nystuen is loaded with the bank address of the previous memory access request. Claims 17 and 21, however, recite assigning a memory request to one of at least one controllers from the plurality of memory requesters not in the grant history register rather than a bank address in memory that was previously accessed. Accordingly, the grant history register in claims 17 and 21 stores requester (origination) information rather than bank address (destination) information. Thus, applicant contends that Nystuen fails to disclose, teach or suggest the step of assigning a memory request to one of the at least one controllers from the plurality of memory requesters not in the grant history register. Further, Shiozaki et al. is devoid of such a feature. For at least this reason, applicant contends that Nystuen and Shiozaki et al. fail to disclose, teach or suggest every feature of claims 17 and 21. Accordingly, applicant contends that claims 17 and 21 are allowable and respectfully request withdrawal of the rejection.

Claims 2-6, 8, 10-14, 16, 18, and 22 include all the features of the independent claim from which they ultimately depend. Thus, applicant contends claims 2-6, 8, 10-14, 16, 18, and 22 are also allowable over the cited references for at least the reasons set forth above with respect to independent claims 1, 9, 15, 17, and 21. Accordingly, applicant respectfully requests that the rejection of claims 2-6, 8, 10-14, 16, 18, and 22 be withdrawn.

Applicant acknowledges with appreciation the Examiner's finding that dependent claims 7, 13, 19, and 20 include allowable subject matter and would be allowed if rewritten in independent form. Applicant submits, however, that there is no need to rewrite these claims in order to place them in condition for allowance because these claims are either directly or indirectly dependent on one of claims 1, 9, and 17, which for the reasons discussed above are in condition for allowance.

In view of the amendments and remarks set forth above, applicant respectfully submits that claims 1-22 are in condition for allowance and early notification to that effect is earnestly solicited.

Respectfully submitted,

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SJW/mm

Dated: November 28, 2006

The Director is hereby authorized to charge or credit Deposit Account No. **18-0350** for any additional fees, or any underpayment or credit for overpayment in connection herewith.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on: November 28, 2006

Michele McDevitt

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